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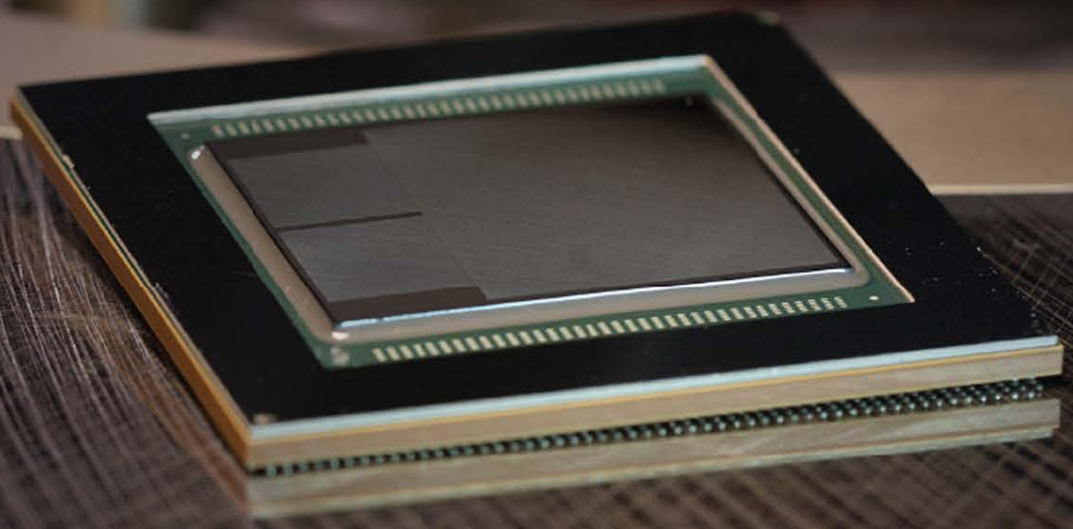

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Wafer-level polymer/metal hybrid bonding using a photosensitive permanent bonding material

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Downscaling is a never-ending task for the semiconductor industry to meet the ever-increasing electronic system demands for higher performance and functionality, smaller system form factor, and lower power consumption and cost. Moore's Law drove the industry for decades to double the number of transistors on a chip with node scaling for 2D device fabrication. However, the development of next-generation silicon node manufacturing becomes more and more challenging and costly because of lithography limitations.

System scaling for 3D device fabrication is an emerging concept for integrating more functional materials along with various semiconductor technologies in a chip, or more chip carrier packages stacked through advanced packaging and manufacturing process technologies [1-2]. Devices with higher bandwidth and with better power and signal integrity can then be achieved in a more economical way through finer-pitch die-to-die interconnection.

Bonding technology offers a z-axis direction of integration playing an important role in realizing 3D device fabrication. Chips or wafers with different functional or process technology can be fabricated separately and then stacked and integrated together by vertical bonding integration. The hybrid bonding technology, based on metal-to-metal and dielectric-to-dielectric bonding simultaneously with the die-to-die interconnection pitch shrinking down to sub-10µm has proven to be an effective way to enhance performance and density of die-to-die interconnects and can be used extensively in many computing and memory applications in the future [3].

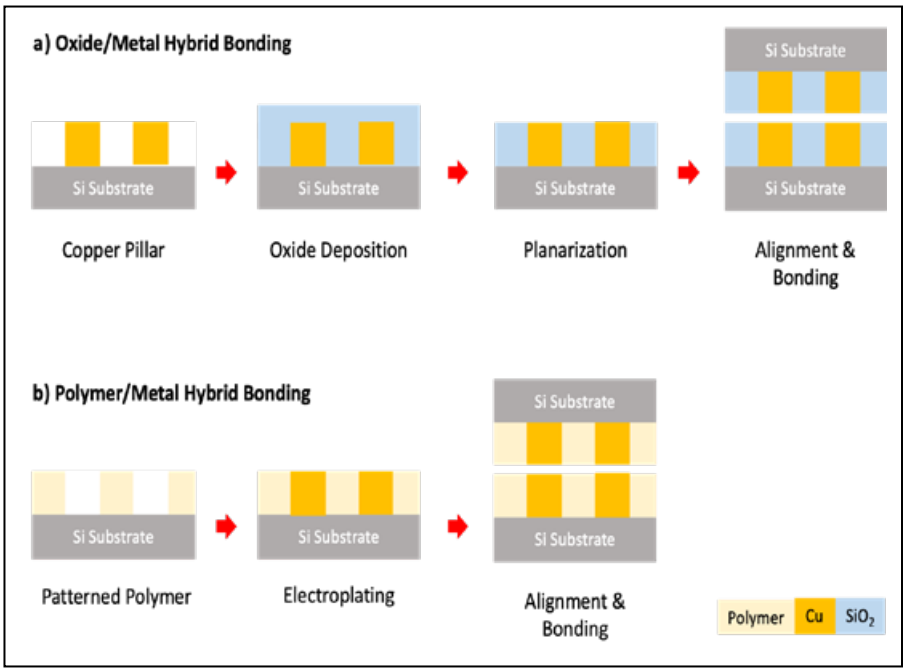

Figure 1: Process flow for wafer-level hybrid bonding using a) oxide, and b) polymer as a dielectric.

Dielectric/metal hybrid bonding

Conventional hybrid bonding uses silicon dioxide as a dielectric to fill up the interspace between micro-interconnections to enhance bond strength and reliability. Also, it can prevent metal oxidation during the bonding process. **Figure 1a** illustrates the process flow for the use of inorganic oxide as a dielectric for the oxide/metal hybrid bonding. However, there are some issues using silicon oxide for hybrid bonding. First, silicon oxide has poor stress absorption because of its high modulus and the hardness of silicon oxide makes it difficult to flow or deform in the bonding interface. As a result of these challenges, using silicon oxide requires an extra chemical mechanical polishing (CMP) process before bonding to ensure the bond interface is extremely flat (~1nm) to achieve a successful bonding.

Polymeric bonding material has a lower modulus than inorganic silicon oxide, and has been widely used in many fields of wafer-level bonding. Polymeric bonding materials exhibit good bond-line quality and excellent tolerance to surface topography [4]. The use of a polymeric bonding material as a dielectric layer provides several advantages including: 1) the polymer can flow better compared to oxide to fill air gaps between metal wires or pads during the bonding process and results in improvements to the quality and reliability of the bonded stack. Additionally, 2) the CMP process for the surface planarization prior to bonding could possibly be skipped with a better bonding capability and bonding strength from the polymeric bonding material. **Figure 1b** shows the process flow for using polymer as a dielectric for the polymer/metal hybrid bonding. However, the concern for using polymeric bonding material is that most of the polymer dielectric materials require 300°C or higher temperature for curing, which will limit the type of metals that can

be used and the thermal budget for the overall processes.

In this paper, a wafer-level polymer/metal hybrid bonding is demonstrated by using a developmental low-curing-temperature photosensitive permanent bonding material as the dielectric. Therefore, the thermal budget of the integration process can be controlled at 250°C. In addition, the merits of the photosensitive permanent bonding material including low dielectric constant and dissipation factor, superior thermal stability, low processing and curing temperatures, and excellent bonding strength, make it an attractive candidate for the future development of polymer/metal hybrid bonding to replace the current oxide/metal hybrid bonding.

Mechanical Properties

Cure Temp (°C)	Tensile Strength (MPa)	Elongation (%)	Modulus (MPa)	CTE (ppm/°C)	T_g (°C)	T_d (°C)	Moisture Uptake (%)	Thermal Conductivity (W/mK)
180	12.4	112	171	157	85	373	0.02	0.25

Electrical Properties

Dielectric Constant (10 GHz)	Dissipation Factor (10 GHz)	Breakdown Voltage (V/µm)	Volume Resistivity (Ω-cm)
2.6	0.0016	TBD	6.99×10^{16}

Reliability Test

THST (85°C/85% 96 hr)	TCT	b-HAST
Pass	TBD	TBD

Table 1: Material properties of photosensitive permanent bonding material (PS PBM).

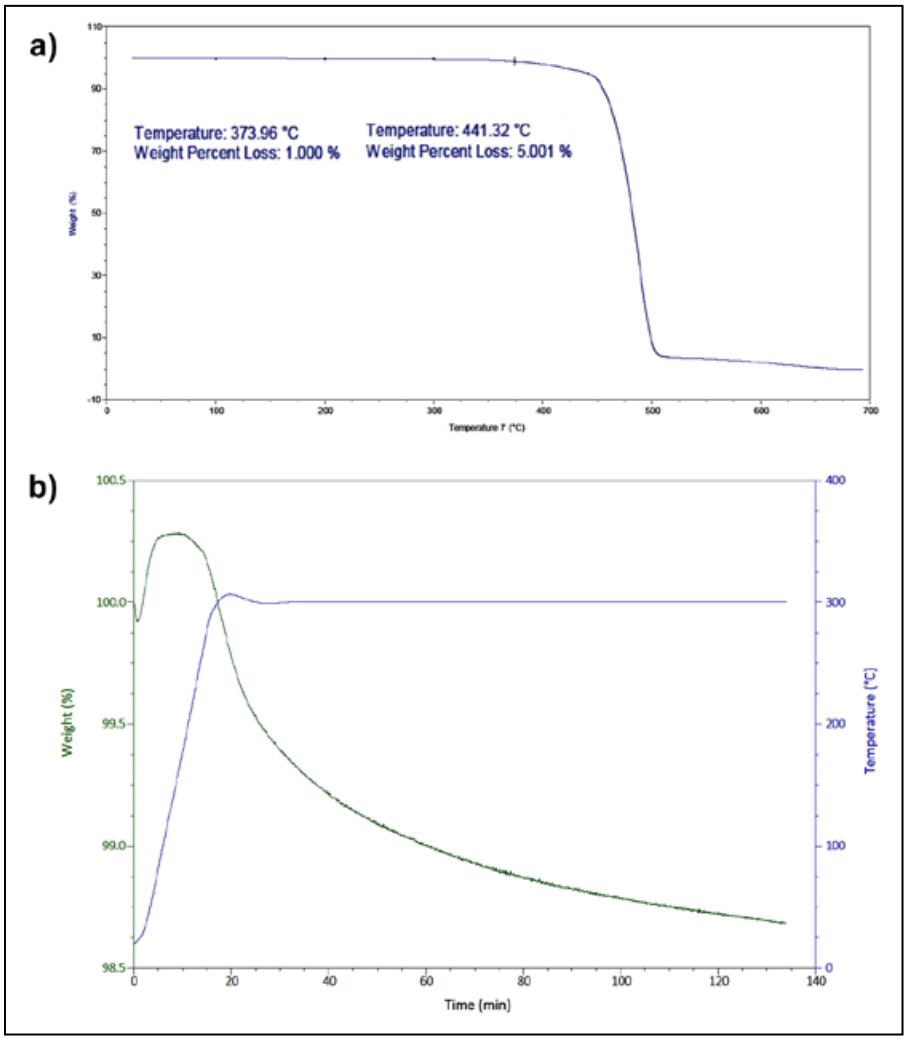

Figure 2: a) Ramp and b) isothermal TGA scan images for PS PBM under nitrogen (with a ramp of 10°C/min).

Photosensitive permanent bonding material (PS PBM)

A developmental photosensitive permanent bonding material (PS PBM) is proposed by Brewer Science, Inc. for the polymer/metal hybrid bonding application. The PS PBM can be coated at various film thicknesses, ranging from 3µm to 20µm in a single coat, which is good to cover most bumps or other surface topographies without causing much stress on the wafer stack.

Compared to most polymeric bonding materials, which require 300°C or higher for curing, the cure temperature for the PS PBM is only 180°C, allowing the thermal budget of the integration process to be greatly reduced. As a dielectric, the PS PBM possesses a low dielectric constant of 2.5 and a dissipation factor of 0.0016 at a frequency of 10GHz. The low Young's modulus and high elongation ensure it has the ability to absorb thermally-induced stress created during thermal processes, resulting in minimal bowing of the bonded substrates. The general mechanical, electrical, and reliability properties of the PS PBM are summarized in Table 1. The points outlined above are discussed in the sections below.

Thermal stability. The thermal stability of the PS PBM is evaluated using ramp and isothermal thermogravimetric analysis (TGA) (see Figure 2). The result shows the PS PBM has a good thermal stability with 1% weight loss at 373°C and a 5% weight loss up to 441°C in a nitrogen atmosphere. The isothermal TGA for the PS PBM heated at 300°C for 2 hours in nitrogen shows there is only about a 1% weight loss during thermal processing. The excellent thermal stability of the PS PBM ensures it has a good thermal budget, which is required for metal annealing and other thermal processes used for hybrid bonding.

Patterning performance. The PS PBM is designed as negative tone and sensitive to i-line (365nm) light sources. To demonstrate the patterning capability,

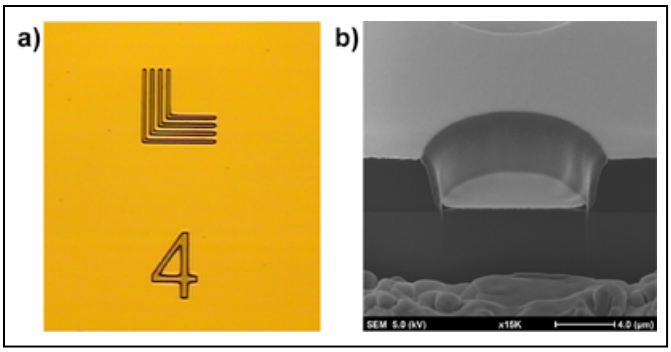

Figure 3: Patterning capability of PS PBM: with a) a microscope; and b) cross-section SEM inspections.

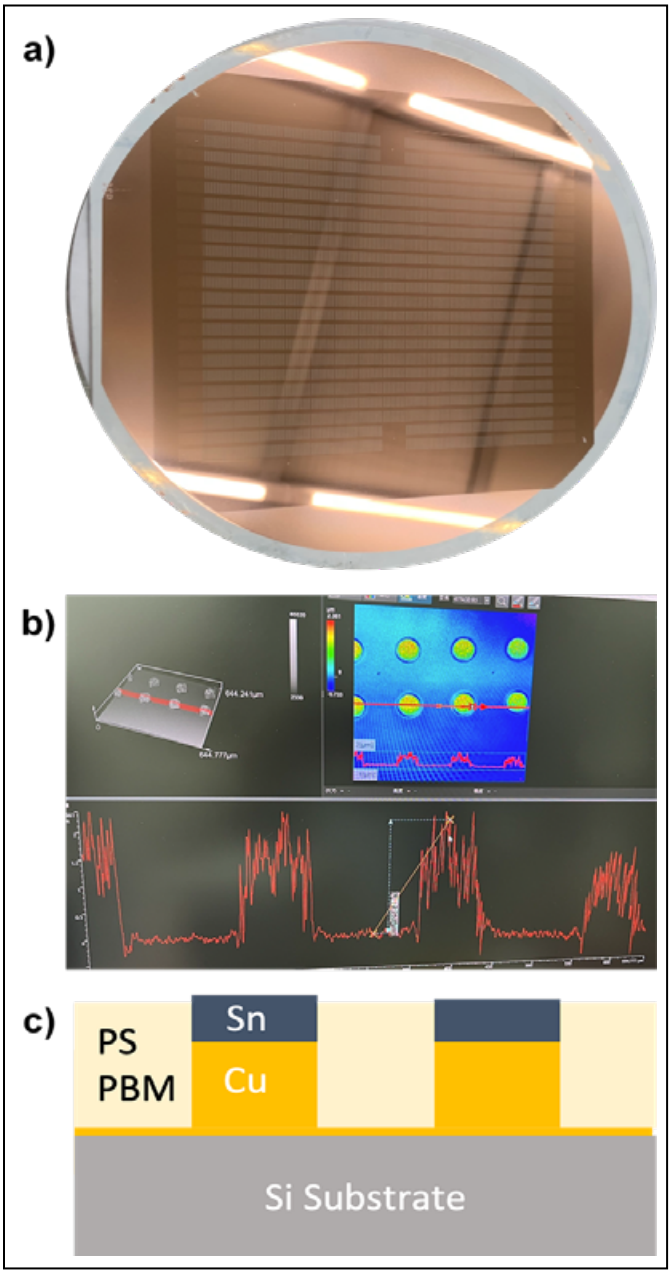

Figure 4: a) A patterned PS PBM wafer with electroplated Cu-Sn; b) a microscope image of a Cu-Sn bump; and c) a schematic of the structure.

a 5µm-thick film of the PS PBM was spin-coated onto a 100mm wafer. The wafers were contact-baked on hot plates at 60°C for 5 minutes and 120°C for an additional 10 minutes for soft bake. Exposure was conducted by an i-line mask aligner at an exposure energy of 100mJ/cm^2. The wafer was then developed using a puddle develop process with cyclopentanone as the developer. Figure 3 shows the fine-pitch patterning capability of the PS PBM for a 4µm line/space feature with a 5µm thickness PS PBM film (based on microscope inspection) and a steep sidewall angle (~90°) based on a cross-section measured using a scanning electron microscope (SEM) on a 10µm via pattern.

Cu-Sn electroplating. A silicon wafer with a patterned PS PBM was fully cured at 200°C for 1 hour for the metallization with electroplating. A Cu-Sn metal stack was selected for bonding because of the low metal annealing temperature at 250°C. A critical condition for the experiment is the metal height design and control because there is no surface planarization applied before the wafer-level bonding. In this study, we used Cu-Sn bumps with 2µm-thick Sn and 4µm-thick Cu electroplated on the patterned wafer with the thickness of the PS PBM film being 5µm. The Cu-Sn electroplated PS PBM wafer, its microscope image, and the schematic structure are shown in Figure 4.

PS PBM/Cu-Sn hybrid bonding. Finally, two PS PBM patterned silicon wafers with Cu-Sn plated metals were bonded together without CMP for surface planarization. The wafer-level hybrid bonding was conducted at 250°C for 60min with a bonding pressure of 20kN to form an interconnection between the layers. The bonded wafer pair was further analyzed by

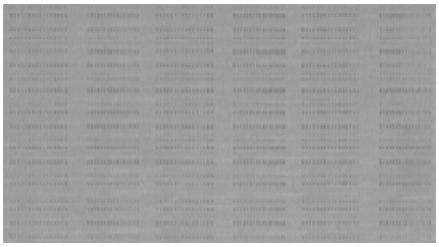

Figure 5: An SAT image of the metal interconnects area for a PS PBM/Cu-Sn bonded stack.

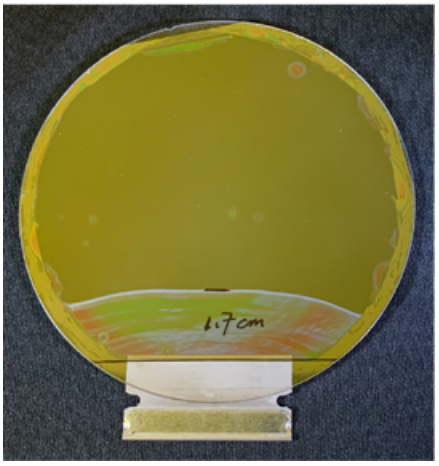

Figure 6: Wafer-level Maszara bond strength test.

scanning acoustic tomography (SAT) to inspect the bonding quality. **Figure 5** shows a magnified view of the SAT image focused on the metal interconnects area, which demonstrates a good bond line quality with no voids on both the PS PBM interfaces (light gray area) and the metal-to-metal contacts (dark gray area).

Bond strength. Silicon wafers coated with the PS PBM were bonded together to evaluate the bond strength of the polymeric bonding material. The bonding was carried out at 150°C, 8kN, for 15min. The temperature used for bonding the PS PBM itself is much lower than the temperature for PS PBM/Cu-Sn hybrid bonding because there is no metal annealing required. Actually, the PS PBM can be bonded at <100°C, or even room temperature. A detailed study will be published in a separate paper at the Electronic Components and Technology Conference (ECTC) later this year.

The bond strength was evaluated with a Maszara razor blade test at wafer-level [5-6] with the PS PBM in a fully-cured state before bonding. The test is performed by inserting a razor blade between the bonded PS PBM wafer pairs, and then measuring the resulting crack length via visual or infrared inspection. **Figure 6**

shows the razor blade test on a silicon-to-glass configuration with a measured crack length of 17mm. The corresponding bond strength was determined using the Maszara model to be >2.5J/m^2, which is greater than the bulk fracture strength of silicon. These results indicate the PS PBM has the strong bond strength required for hybrid bonding and is better than bonding with inorganic silicon oxide or silicon carbon nitride as the dielectric (0.9-1.8Jm^2) [7].

Summary

This paper introduces a developmental photosensitive permanent bonding material with features of a low dielectric constant and dissipation factor, superior thermal stability, and low processing and curing temperatures.

The fine-pitch patterning capability of the PS PBM is also shown, supporting its use for dense die-to-die interconnection. With proper design and control in metal height, the PS PBM/Cu-Sn structure has demonstrated a good wafer-level hybrid bonding quality between metal-to-metal and between polymer-to-polymer interfaces without CMP processing for surface planarization. The bond strength for the PS PBM was then evaluated to be stronger than using silicon oxide as the dielectric. More evaluations such as grinding, reliability, and electrical performance for the hybrid bonded stack with PS PBM will be conducted and shared in the future.

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Biographies

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Component-level gap height between LSC and collapsed BGA solder ball

As a continuation to the aforementioned SMT process corner investigation, quantifying the LSC process capability to the collapsed BGA solder ball gap height after the FCBGA assembly process was studied. High LSC process control to the collapsed BGA solder ball clearance is a prerequisite to a robust SMT assembly process to ensure no defects manifest associated with LSC clearance with the PCB after mounting (to the PCB). As such, gap height measurements between the LSC and BGA solder ball were evaluated across multiple assembly lots to determine if Cpk values meet automotive requirements, i.e., ≥1.67.

Figure 8 is a simplified illustration of the gap height measurement between the LSC and the collapsed BGA solder ball being investigated on the flip-chip substrate after the FCBGA assembly process. The target minimum gap height is greater or equal to 130µm. To prove a high assembly process margin, gap height measurements between the LSC and the BGA solder ball were performed on 100% of the units across three assembly lots using standard ball

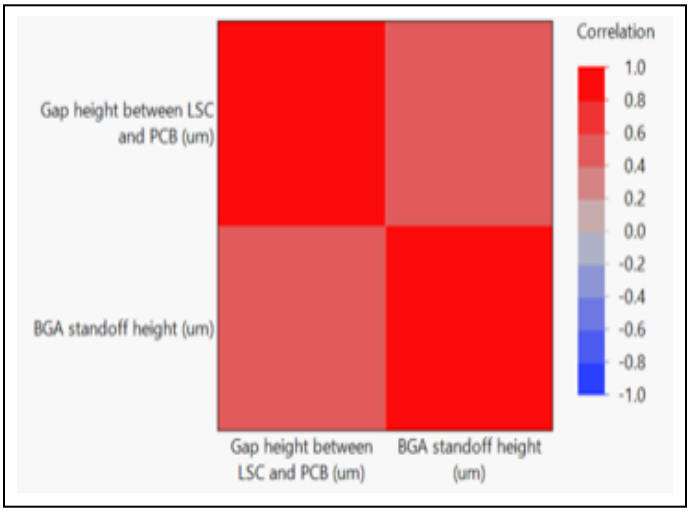

Figure 7: Color map showing a moderate positive correlation between the gap height between a LSC and a PCB and between the BGA standoff height.

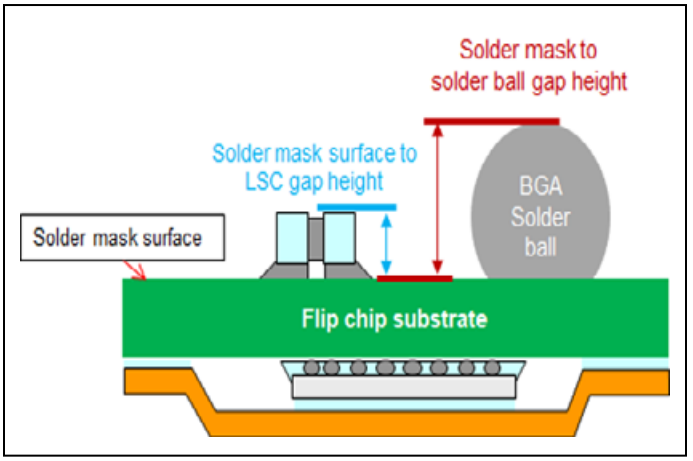

Figure 8: Dead-bug illustration of a LSC to a collapsed BGA solder ball gap height measurement.